

Please substitute the following amended claim(s) for corresponding claim(s) previously presented. A copy of the amended claim(s) showing current revisions is attached.

1. (Amended) A semiconductor memory comprising:
a first conductivity type semiconductor substrate; and
one or more memory cells comprising an island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being
formed to entirely or partially encircle a sidewall of the island-like semiconductor layer,
wherein an active region of at least one of said memory cells is electrically insulated from the semiconductor substrate.

2. (Amended) A semiconductor memory according to claim 1, wherein said active region of said at least one memory cell is electrically insulated from the semiconductor substrate by a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer, or by a second conductivity type impurity diffusion layer and a first conductivity type impurity diffusion layer formed in the second conductivity type impurity diffusion layer.

33 4. (Amended) A semiconductor memory according to claim 1, wherein the active region of said memory cell is electrically insulated from the semiconductor substrate by:

a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer and

a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the island-like semiconductor layer.

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5. (Amended) A semiconductor memory according to claim 1, wherein a plurality of memory cells are formed with regard to one island-like semiconductor layer, and an active region of at least one of the memory cells is electrically insulated from another memory cell by a second conductivity type impurity diffusion layer formed in the semiconductor substrate or the island-like semiconductor layer and a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the island-like semiconductor layer.

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13. (Amended) A semiconductor memory according to claim 1, wherein a plurality of memory cells are formed with regard to one island-like semiconductor layer, and an electrode for electrically connecting channel layers of memory cells is further formed between control gates.

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19. (Amended) A semiconductor memory according to claim 1, wherein a lower gate electrode of a selection transistor, the control gate of the memory cell, and an upper

B5 gate electrode of another selection transistor are arranged in an upward order in a direction vertical to the semiconductor substrate.

Please add the following new claims:

B6 29. (New) The semiconductor memory of claim 1, wherein the control gate and the charge store layer each laterally surround a portion of the sidewall of the island-like semiconductor layer on all lateral sides thereof.

30. (New) The semiconductor memory of claim 1, wherein the active region of the one memory cell is electrically insulated from the semiconductor substrate by at least one diffusion layer which is formed at a bottom portion of the island-like semiconductor layer.

31. (New) The semiconductor memory of claim 1, wherein the active region of the one memory cell is electrically insulated from the semiconductor substrate by at least a diffusion layer formed in a top portion of the semiconductor substrate immediately under the island-like semiconductor layer.

32. (New) The semiconductor memory of claim 1, wherein the island-like semiconductor layer is pillar-shaped so as to have a height dimension greater than a width dimension.

33. (New) The semiconductor memory of claim 32, wherein the island-like semiconductor layer has a circular cross section when viewed from above.

34. (New) The semiconductor memory of claim 1, wherein the semiconductor memory is an EEPROM.

35. (New) The semiconductor memory of claim 1, wherein said sidewall of the island-like semiconductor layer is vertically extending relative to a surface of the semiconductor substrate.

36. (New) A semiconductor memory comprising:

a first conductivity type semiconductor substrate;

at least one memory cell comprising an island-like semiconductor layer, a charge storage layer and a control gate, wherein the charge storage layer and the control gate entirely or partially laterally surround at least a portion of a sidewall of the island-like semiconductor layer; and

wherein an active region of said memory cell is electrically insulated from the semiconductor substrate.

37. (New) A semiconductor memory according to claim 36, wherein said active region of said memory cell is electrically insulated from the semiconductor substrate by

at least a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer.

38. (New) A semiconductor memory according to claim 36, wherein the active region of said memory cell is electrically insulated from the semiconductor substrate by:

a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer, and

Bp a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the island-like semiconductor layer.

39. (New) The semiconductor memory of claim 36, wherein the control gate and the charge store layer each laterally surround at least said portion of the sidewall of the island-like semiconductor layer on all lateral sides thereof.

40. (New) The semiconductor memory of claim 36, wherein the active region of the memory cell is electrically insulated from the semiconductor substrate by at least one diffusion layer which is formed at a bottom portion of the island-like semiconductor layer.

41. (New) The semiconductor memory of claim 36, wherein the island-like semiconductor layer is pillar-shaped so as to have a height dimension greater than a width dimension.

42. (New) The semiconductor memory of claim 41, wherein the island-like semiconductor layer has a circular cross section when viewed from above.

B6 43. (New) The semiconductor memory of claim 36, wherein the semiconductor memory is an EEPROM.

44. (New) The semiconductor memory of claim 36, wherein said sidewall of the island-like semiconductor layer is vertically extending relative to a surface of the semiconductor substrate.

45. (New) The semiconductor memory of claim 36, wherein a plurality of memory cells are stacked on top of one another over the semiconductor substrate and each use the island-like semiconductor layer, and wherein respective active regions of each of the memory cells are electrically insulated from the semiconductor substrate.

46. (New) A semiconductor memory comprising:
a first conductivity type semiconductor substrate;

at least one memory cell comprising a pillar-shaped semiconductor layer having a height dimension greater than a width dimension, a charge storage layer and a control gate, wherein the charge storage layer and the control gate entirely or partially laterally surround at least a portion of a sidewall of the pillar-shaped semiconductor layer, wherein the sidewall of the pillar-shaped semiconductor layer extends vertically relative to the semiconductor substrate; and

wherein at least a portion of the pillar-shaped semiconductor layer of the memory cell is electrically insulated from the semiconductor substrate.

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47. (New) A semiconductor memory according to claim 46, wherein said portion of the pillar-shaped semiconductor layer is electrically insulated from the semiconductor substrate by at least a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the pillar-shaped semiconductor layer.

48. (New) A semiconductor memory according to claim 46, wherein said portion of the pillar-shaped semiconductor layer is electrically insulated from the semiconductor substrate by:

a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the pillar-shaped semiconductor layer, and

a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the pillar-shaped semiconductor layer.

49. (New) The semiconductor memory of claim 46, wherein the control gate and the charge store layer each laterally surround at least said portion of the sidewall of the pillar-shaped semiconductor layer on all lateral sides thereof.

B6 50. (New) The semiconductor memory of claim 46, wherein the pillar-shaped semiconductor layer has a circular cross section when viewed from above.

51. (New) The semiconductor memory of claim 46, wherein the semiconductor memory is an EEPROM.

52. (New) The semiconductor memory of claim 46, wherein a plurality of memory cells are stacked on top of one another over the semiconductor substrate and each use the pillar-shaped semiconductor layer, and wherein respective active regions of each of the memory cells are electrically insulated from the semiconductor substrate.

REMARKS

This is in response to the Office Action dated January 21, 2003. Non-elected claims 20-28 have been canceled, without prejudice in view of the Restriction Requirement. New claims 29-52 have been added. Thus, claims 1-19 and 29-52 are now pending. Attached hereto is a marked-up version of the changes made to the